WHAT IS CLAIMED IS:

1. A method of forming a power semiconductor device comprising the steps of:

A. providing a substrate of a first conductivity type;

B. forming a voltage sustaining region on said substrate by:

1. depositing an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;

2. forming at least one terraced trench in said epitaxial layer, said terraced trench having a plurality of portions that differ in width to define at least one annular ledge therebetween;

3. depositing a barrier material along the walls and bottom of said trench;

4. implanting a dopant of a second conductivity type through the barrier material lining said at least one annular ledge and said trench bottom and into adjacent portions of the epitaxial layer;

5. diffusing said dopant to form at least one annular doped region in said epitaxial layer and at least one other region located below said annular doped region in said epitaxial layer;

6. depositing a filler material in said terraced trench to substantially fill said terraced trench; and

C. forming over said voltage sustaining region at least one region of said second conductivity type to define a junction therebetween.

2. The method of claim 1 wherein the step of forming said at least one terraced trench includes the steps of successively etching the plurality of portions of the terraced trench beginning with a largest width portion and ending with a smallest width portion.

3. The method of claim 2 wherein said smallest width portion is located at a depth in said epitaxial layer such that it is closer to the substrate than the largest width portion.

4. The method of claim 1 wherein said plurality of portions of the terraced trench are coaxially located with respect to one another.

5. The method of claim 1 wherein said plurality of portions of the terraced trench includes at least three portions that differ in width from one another to define at least two annular ledges and said at least one annular doped region includes at least two annular doped regions.

6. The method of claim 4 wherein said plurality of portions of the terraced trench includes at least three portions that differ in width from one another to define at least two annular ledges and said at least one annular doped region includes at least two annular doped regions.

7. The method of claim 6 wherein the step of forming at least one terraced trench includes the steps of successively etching said at least three portions of the terraced trench beginning with a largest width portion and ending with a smallest width portion.

8. The method of claim 7 wherein said smallest width portion is located at a depth in said epitaxial layer such that it is closer to the substrate than said largest width portion.

9. The method of claim 1 wherein step (C) further includes the steps of:

forming a gate conductor above a gate dielectric region;

forming first and second body regions in the epitaxial layer to define a drift region therebetween, said body regions having a second conductivity type;

forming first and second source regions of the first conductivity type in the

first and second body regions, respectively.

10. The method of claim 1 wherein said barrier material is an oxide material.

11. The method of claim 10 wherein said oxide material is silicon dioxide.

12. The method of claim 1 wherein said epitaxial layer has a given thickness and further comprising the step of etching a first portion of the terraced trench by an amount substantially equal to 1/(x+1) of said given thickness , where x is equal to or greater than a prescribed number of annular doped regions to be formed in the voltage sustaining region.

13. The method of claim 1 wherein said material filling the trench is a dielectric material.

14. The method of claim 13 wherein said dielectric material is silicon dioxide.

15. The method of claim 13 wherein said dielectric material is silicon nitride.

16. The method of claim 1 wherein said dopant is boron.

17. The method of claim 9 wherein said body regions include deep body regions.

18. The method of claim 1, wherein said terraced trench is formed by providing a masking layer defining at least a first of said plurality of portions and etching said first portion defined by the masking layer

19. The method of claim 18 further comprising the step of depositing an oxide layer of prescribed thickness along the walls of said first portion of the terraced trench.

20. The method of claim 19 wherein said oxide layer serves as a second masking layer and further comprising the step of etching a second portion of the terraced trench defined by the second masking layer through a bottom surface of the first portion of the terraced trench.

21. The method of claim 20 wherein said prescribed thickness of the oxide layer is selected so that a surface area of the annular ledge and the non-annular region are substantially equal to one another.

22. The method of claim 9, wherein said body region is formed by implanting and diffusing a dopant into the substrate.

23. The method of claim 1 wherein said power semiconductor device is selected from the group consisting of a vertical DMOS, V-groove DMO, and a trench DMOS MOSFET, an IGBT, and a bipolar transistor.

24. A power semiconductor device made in accordance with the method of claim 1.

25. A power semiconductor device made in accordance with the method of claim 7.

26. A power semiconductor device made in accordance with the method of claim 9.

27. A power semiconductor device comprising:

a substrate of a first conductivity type;

a voltage sustaining region disposed on said substrate, said voltage sustaining region including:

an epitaxial layer having a first conductivity type;

at least one terraced trench located in said epitaxial layer, said terraced trench having a plurality of portions that differ in width to define at least one annular ledge therebetween;

at least one annular doped region having a dopant of a second conductivity type, said annular doped region being located in said epitaxial layer below and adjacent to said annular ledge;

a filler material substantially filling said terraced trench; and

at least one active region of said second conductivity disposed over said voltage sustaining region to define a junction therebetween.

28. The device of claim 27 wherein said plurality of portions of the terraced trench includes a smallest width portion and a largest width portion, said smallest width portion being located at a depth in said epitaxial layer such that it is closer to the substrate than a largest width portion.

29. The device of claim 28 wherein said plurality of portions of the terraced trench are coaxially located with respect to one another.

30. The device of claim 27 wherein said plurality of portions of the terraced trench includes at least three portions that differ in width from one another to define at least two annular ledges and said at least one annular doped region includes at least two annular doped regions.

31. The device of claim 29 wherein said plurality of portions of the terraced trench includes at least three portions that differ in width from one another to define at least two annular ledges and said at least one annular doped region includes at least two annular doped regions.

32. The device of claim 27 wherein said epitaxial layer has a given thickness and further comprising the step of etching a first portion of the terraced trench by an amount substantially equal to $1/(x+1)$ of said given thickness , where x is equal to

or greater than a prescribed number of annular doped regions to be formed in the voltage sustaining region.

33. The device of claim 27 wherein said material filling the trench is a dielectric material.

34. The device of claim 33 wherein said dielectric material is silicon dioxide.

35. The device of claim 34 wherein said dielectric material is silicon nitride.

36. The device of claim 27 wherein said dopant is boron.

37. The device of claim 31 wherein a surface area of the at least two annular ledges are substantially equal to one another.

38. The device of claim 27 wherein said at least one active region further includes:

a gate dielectric and a gate conductor disposed above said gate dielectric;

first and second body regions located in the epitaxial layer to define a drift region therebetween, said body regions having a second conductivity type; and

first and second source regions of the first conductivity type located in the first and second body regions, respectively.

39. The device of claim 38 wherein said body regions include deep body regions.

40. The device of claim 27 wherein said terraced trench has a circular cross-section.

41. The device of claim 27 wherein said terraced trench has a cross-sectional shape selected from the group consisting of a square, rectangle, octagon, and a hexagon.